Fabrication of Low Power, High-Speed GaAs LSI On-Board Baseband Switching Matrix

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ABSTRACT

A GaAs LSI On-Board Baseband Switching Matrix (BSM) for use in satellite communications for time-division multiple access (TDMA) system, has been designed and fabricated by using low dissipated Buffered-FET-Logic(BFL) with one level- shifting diode with the FET threshold voltage of about -0.5 V. For a 120 Mbit/s rate traffic signal to be used for TDMA, complete connectivity was confirmed for any possible switching pattern with a fast rise/fall time of about 1 ns at a power dissipation of 160 mW. The switch size is 16x4, expandable up to 16x16 by interbonding.

INTRODUCTION

A GaAs LSI On-Board Baseband Switching Matrix (BSM) for use in satellite communications for 120 Mbit/s time-division multiple access (TDMA) system, has been designed and fabricated in order to assure that the GaAs material is superior to that of Si in considering space applications from view points of radiation hardness, high-speed and low power dissipation.

As previously reported,[1][2] Buffered-FET-Logic (BFL) gate with one level-shifting diode, constructed with depletion type FETs of the threshold voltage reduced down to around -0.5 V, has been successfully adopted for obtaining low power dissipation without any sacrifice of high speed performance by means of design optimization for a high f_T operation.

Fig.1 shows a fundamental BFL NOR gate circuit used for the BSM LSI. The gate width Wb for the active load FET was designed to be half of that Wa for the switching FET to obtain a wide range of high gain transition of about 6 as well as a symmetrical DC noise margin in the inverter section. Also, the gate width ratio of Wc for the source-follower over Wd for the current-source FETs, was chosen to be 1/2 after especially taking into consideration driving ability for fan-out loading.

Fig.2 shows a register circuit, implemented by using a kind of master-slave flip-flop made of the BFL NOR gates. Switching matrix address data, applied to L0~L3, come to finally be stored in the slave flip-flop by way of the master flip-flop through triggering by a negative-going pulse at LD0~LD3 and T. In discussing the IC design feasibility, it is important to investigate whether the gate configuration could give sufficient tolerance for IC dynamic performances and could consequently result in correct operation under some circumstance of dispersion in device parameters. A statistical analysis using Monte Carlo simulation by SPICE II program, was applied to a register circuit shown in Fig.2. The 3σ values(σ :standard deviation) for device parameters, Vth, β, λ and Is in the simulation, were derived from the experimental results obtained so far, and each value was set at 40%, 20%, 20%, and 400%, respectively.

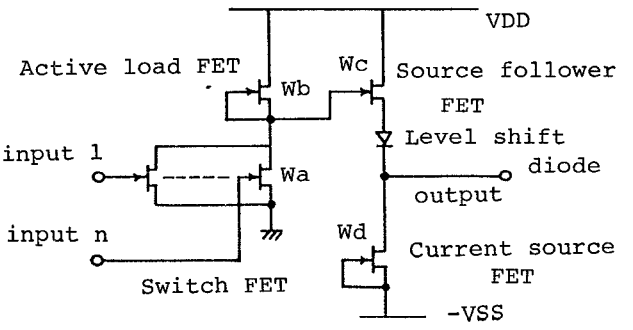

Fig. 1 Basic BFL NOR gate used for the BSM LSI. The number of the level -shifting diodes is reduced to one.

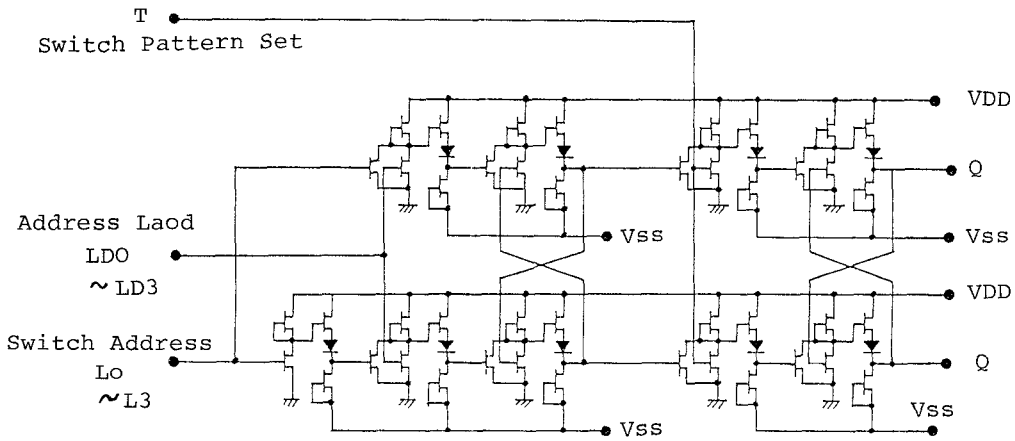

Fig. 2 Register circuit implemented by the BFL NOR gate. The resister is constructed using a master-slave flip-flop.

Fig.3 shows the simulated and evaluated results for output levels of Q and $\overline{Q}$ with Vdd and Vss biased at 2V and -1.5V. The latter case is based upon measurements for register TEGs (Test Element Groups) fabricated on the same wafer as the BSM. They are in reasonable agreement with each other and so assure design accuracy. The histograms illustrate that the average values (V_H=+0.62V and V_T=-0.72V) and the standard deviations (σ_{VH}=0.055 and σ_{VL}=0.095) for high and low levels are allowable for normal operation.

Fig.4 shows a block diagram for the fabricated BSM IC, consisting of a 16x4 switching matrix, 4-bit registers, a wired decoder circuit including 5 input NOR gates and output buffers. Various traffic signals which are simultaneously applied at the inputs, can be transfered to any particular output through the addressing function performed by both the 4 bit register(2^4=16 combinations) and the wired decoder circuit. The 4-bit register has been implemented by adopting 4 master-slave flip-flops in order to prevent a signal scue and to eliminate addressing errors. The switch size is expandable up to 16 inputs x 16 outputs by inter-bonding 4 BSM chips together.

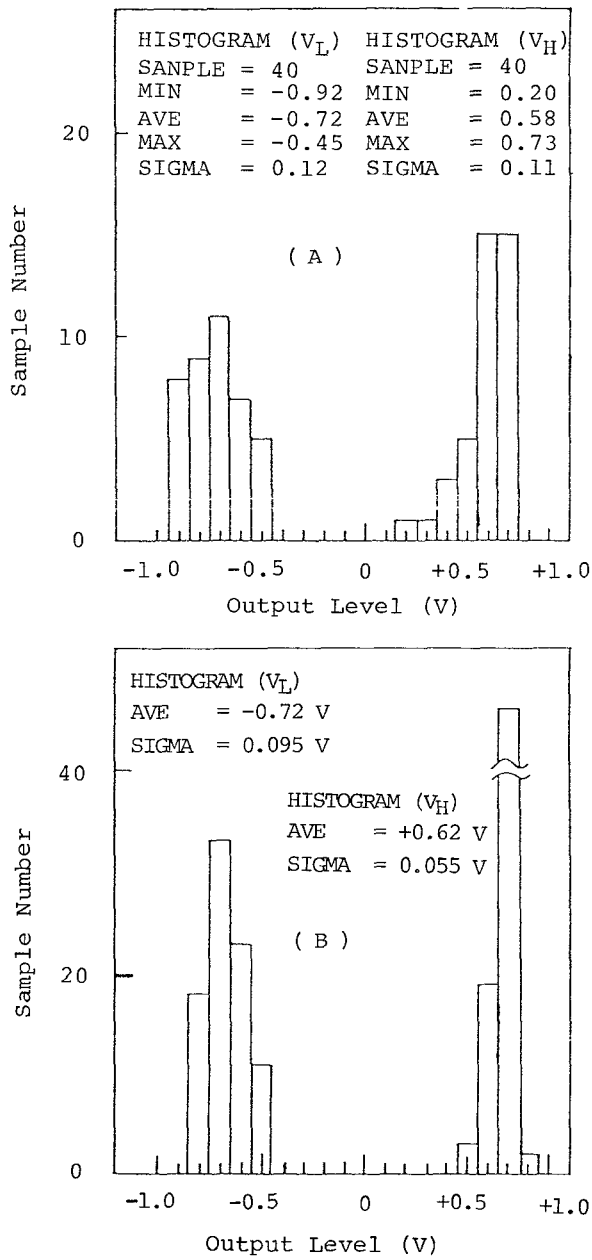

Fig. 3 Histograms of high and low levels for the resister outputs in case of (A)simulation and (B) measurement.

IC FABRICATION

Fig.5 shows a photograph of the fabricated BSM IC, measuring 3.3x2.8 mm^2; 1292 FETs and 212 diodes are integrated in it. The gate width of driving and current source FETs employed in the IC is typically 10 um, except for that of output buffers of 20 um so as to increase driving ability for the long interconnects to the bonding pads. The design rule used is 3 um, that is, minimum value of the line width, the spacing between the interconnects and the size of through holes are 3 um. The active layers of FETs and diodes have been formed by implanting Si^+ into a lightly Cr doped semi-insulating GaAs substrate with an acceleration energy of 50 KeV and a dose of around 2.2×10^{12} cm^{-2}. The FETs have a CSE (Closely Spaced Electrode) structure, where gate to source and gate to drain spacings are diminished down to 0.4 um by utilizing a self-alighnment technology to reduce the series parastic resistances of FETs. The gate of the FET is made of 1.0 um long Al stripe. A typical transconductance of 88mS/mm was obtained for the FET.

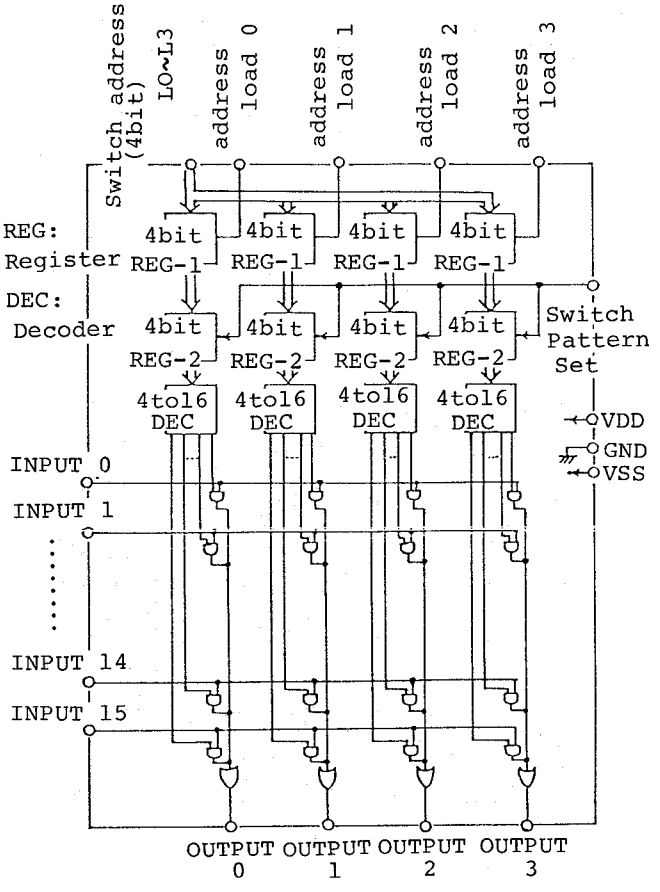

Fig. 4 Block diagram for a GaAs LSI BSM, consisting of registers, decoders and switching gates.

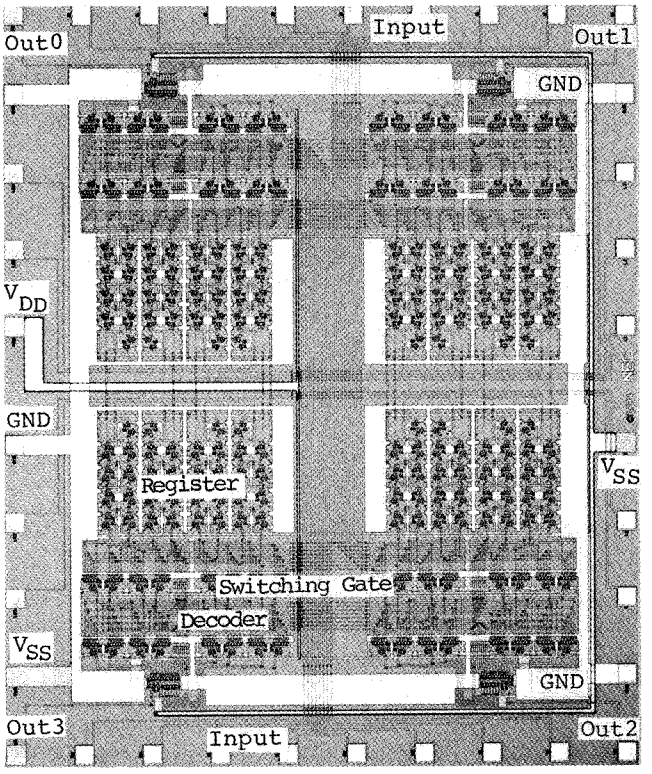

Fig. 5 Photograph of a developed GaAs BSM IC, where 1292 FETs and 212 diodes are integrated.

When the device complexity is increased, the technology for reproducible interconnections becomes indispensable for high yield IC fabrication. To eliminate the potential crossover problems resulting from poor step coverage, a dry etched, planar two- level interconnect was utilized, including a process for leveling the surface of the dielectric layers(SiO_2) on the first interconnect(Al) before the second metal(Ti/Pt/Au) deposition. The second level interconnects are replicated by using ion-milling, with Au on top.

EVALUATION

The evaluation of RF performances was carried out by mounting an IC chip in a 40-lead flat package shown in Fig.6, and by inserting it into a 50Ω microstrip line measurement system. DC bias voltages of 2V for Vdd and -1.5V for Vss were applied. Fig.7 shows output waveforms of channel-0 to channel-3 witout any degradation in the traffic signals of 60 Mbit/s, and also exhibits that the time difference between any of the output signals caused by the BSM is negligibly small. In addition, complete connectivity among 16 inputs and 4 outputs was confirmed for any possible switching patterns.

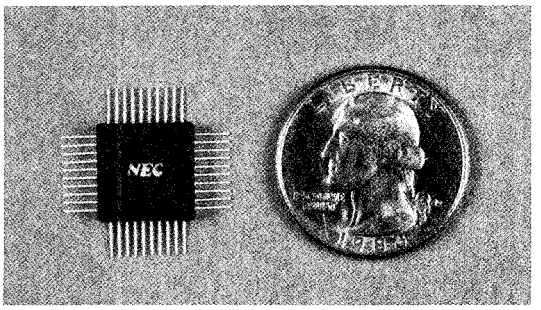

Fig. 6 Photograph of a BSM 40-lead flat package.

The logic levels of the traffic signals obtained are around +0.6V for high level and -0.6V for low level, respectively. Power dissipation was as small as 160 mW, corresponding to 0.8 mW per gate.

Fig.8 shows photographs of leading and falling edges for an output pulse from the BSM IC. In spite of an average 400 um length of interconnects, equivalent to 6 counts of fan-out, fast rise and fall times of about 1.2 ns and 0.6 ns have been realized; this leads to a conclusion that the BSM could operate at the rate of 450 Mbit/s with a margin of 10%. Fig.9 shows a transmission loss and isolation characteristics for a packaged BSM with output signal terminated 50 . Input power level was kept so low as not to bring about the over-drive effect. It can be seen that a switched on/off ratio of more than 30 dB was obtained at the frequency of 300 MHz. However, it begins to roll off with increasing frequency from 400 MHz, resulting in 3dB degradation at about 450 MHz.

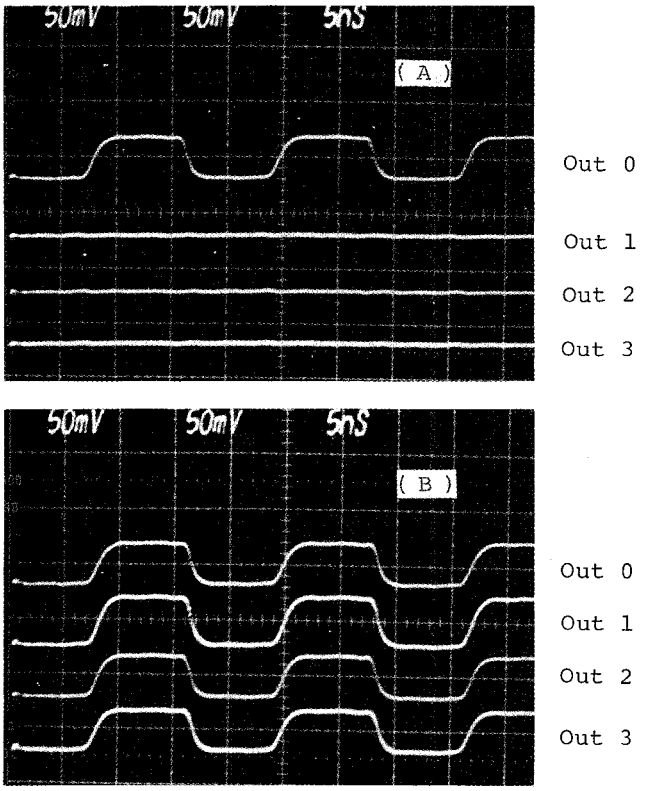

Fig. 7 Output waveforms for a 60 Mbit/s input. (A)Input-0 is connected to output-0 by selecting (0000) as switching address L0,L1,L2,L3 and (0111) as address load 0,1,2, 3. (B)Input-0 is simultaneously connected to output-0, output-1, output-2 and output-3, where (0000) is selected instead of (0111) for address load.

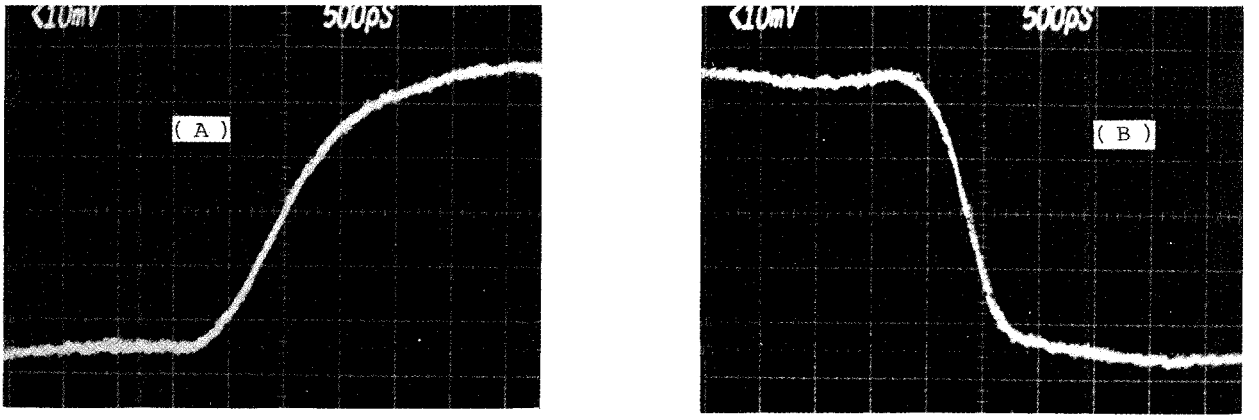

Fig. 8 Enlarged photographs of an output waveform. (A)Leading and (B)falling edges of an output pulse. The rise and fall time are seen to be 1.2 ns and 0.6 ns, respectively.

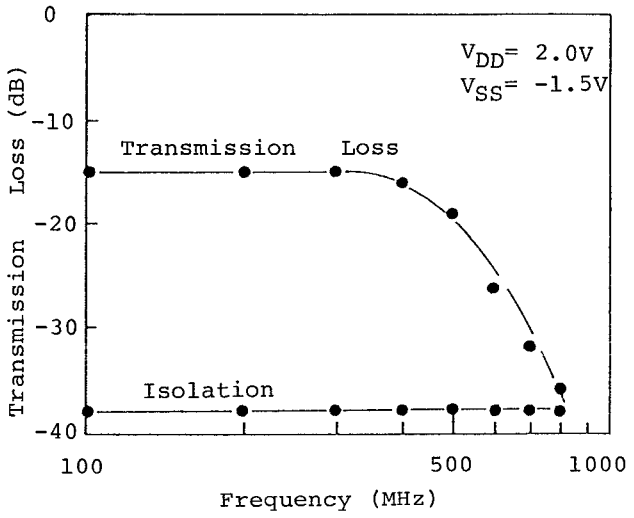

Fig. 9 Transmissionloss versus frequency characteristics for a packaged BSM IC. Vdd and Vss are biased at 2.0V and -1.5V.

Fig.10 shows a BSM temperature characteristic with respect to power dissipation, output logic levels and rise/fall time, where temperature increases from 0°to 50°C. Temperature coefficients of 0.7mW/°C, -3mV/°C, 0.2mV/°C, -0.004ns/°C, and 0.004ns/°C can easily be calculated, suggesting a wide tmeperature range of operation. The increase in power dissipation might be only 50mW when the temperature goes up to 100°C.

CONCLUSION

In conclusion compact, light weight GaAs BSM IC, suitable for satellite communications, has successfully been developed with excellent performance such as high-speed and low power dissipation, and the device feasibility has satisfactorily been demonstrated. With further investigation on reliability characteristics, a promising possibility of establishing a practical TDMA system using BSM ICs could be expected.

References
(1) R.Yamamoto, A.Higashisaka, S.Asai, T.Tsuji, Y.Takayama and S.Yano, "Depletion Type GaAs MSI 32b Adder", ISSCC 83, Digest of Tech.Paper, PP40-41, Feb.1983
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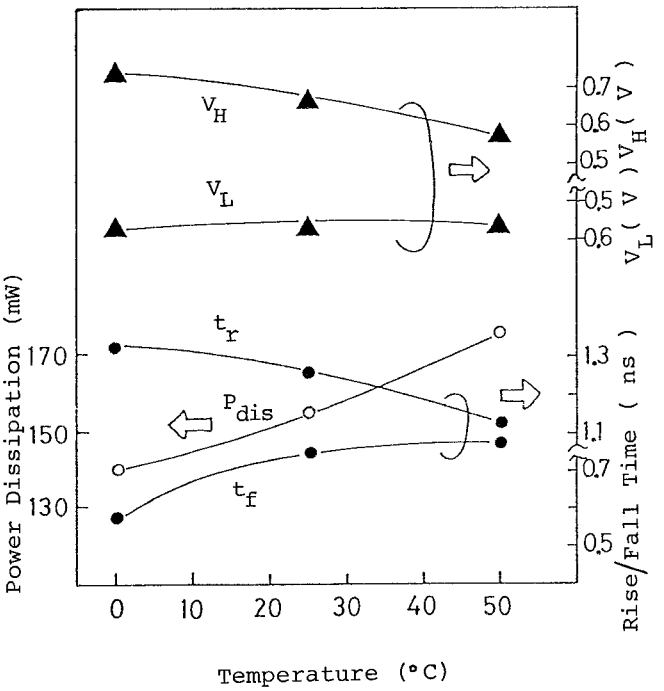

Fig. 10 Dependency of power dissipation, output logic levels and a rise/fall time on temperature, ranging from 0°C to 50°C.

TABLE 1 Characteristics of Baseband Switch Matrix

Item	Measured Value
Switch Configuration	16 x 4 (with Memories) crossbar
Input/Output Traffic Signal	
a) Data Rate	120 Mb/s
b) Logic Level	"High": +0.5V ∿ +0.7V "Low" : -0.5V ∿ -0.7V
c) Rise and Fall Times	0.6 nsec ∿ 1.5 nsec
d) Timing Errors	Within 1 nsec
Control Signal	
a) Drive Level	"High": +0.5V ∿ +0.7V "Low" : -0.5V ∿ -0.7V
Power Consumption	150 mW
Chip Size	2.8mm x 3.32mm
Package Size	12mm x 12mm
Weight	1.2 g